EdSim51DI - Version 2.1.32

System Clock (MHz) 12.0 | 1 | Update Freq.

SBUF

R/O	W/O		TH0	TL0		R7	0x00		B	0x00
0x00	0x00		0x00	0x00		R6	0x00		ACC	0x00
RXD	TXD					R5	0x00		PSW	0x00
1	1		TMOD	0x00		R4	0x00		IP	0x00
SCON	0x00		TCON	0x00		R3	0x00		IE	0x00
						R2	0x00		PCON	0x00
pins	bits		TH1	TL1		R1	0x00		DPH	0x00
0xFF	0xFF	P3	0x00	0x00		R0	0x00		DPL	0x00
0xFF	0xFF	P2							SP	0x07
0xFF	0xFF	P1	PC							
0xFF	0xFF	P0	0x0000							

8051

i | PSW | 0 0 0 0 | 0 0 0 0

Modify RAM

Data Memory | addr 0x00 | 0x00 value

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
50	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Remove All Breakpoints

RST | Assm | Run | New | Load | Save | Copy | Paste | X

U

```
                Org ØØh
ØØØØ| Select:       SetB PØ.7    ;Chip s
ØØØ2|               SetB P3.3    ;Select Disp
ØØØ4|               SetB P3.4    ;Select Disp
ØØØ6| Main:         Mov A,#ØbØh ;Display da
ØØØ8|               Mov P1,A

                End
```

P0.7	1	Display-select Decoder CS|DAC WR
P0.6	1	Keypad Column 2
P0.5	1	Keypad Column 1
P0.4	1	Keypad Column 0
P0.3	1	Keypad Row 3
P0.2	1	Keypad Row 2
P0.1	1	Keypad Row 1
P0.0	1	Keypad Row 0
P1.7	1	LED 7|Seg. dp|DAC DB7|LCD DB7
P1.6	1	LED 6|Seg. g|DAC DB6|LCD DB6
P1.5	1	LED 5|Seg. f|DAC DB5|LCD DB5
P1.4	1	LED 4|Seg. e|DAC DB4|LCD DB4
P1.3	1	LED 3|... d|..DB3|..DB3|.. RS
P1.2	1	LED 2|... c|..DB2|..DB2|LCD E
P1.1	1	LED 1|Seg. b|DAC DB1|LCD DB1
P1.0	1	LED 0|Seg. a|DAC DB0|LCD DB0
P2.7	1	SW 7|ADC DB7
P2.6	1	SW 6|ADC DB6
P2.5	1	SW 5|ADC DB5
P2.4	1	SW 4|ADC DB4
P2.3	1	SW 3|ADC DB3
P2.2	1	SW 2|ADC DB2
P2.1	1	SW 1|ADC DB1
P2.0	1	SW 0|ADC DB0
P3.7	1	ADC RD|Comparator Output
P3.6	1	ADC WR
P3.5	1	Motor Sensor
P3.4	1	Display-select Input 1
P3.3	1	AND Gate Output|Display-se..t 0
P3.2	1	ADC INTR
P3.1	1	Motor Control Bit 1|Ext. UART Rx
P3.0	1	Motor Control Bit 0|Ext. UART Tx

DI | i | LD

7 6 5 4 3 2 1 0

1 2 3 | AND Gate Disabled
4 5 6 | Key Bounce Disabled
7 8 9 | Standard | i
* 0 #

U | No Parity | 8-bit UART @ 4800 Baud
Rx | Rx Reset
Tx | Tx Send | i

0.0 V output
Scope
DAC

BF | AC | IR | DR | i

8.8.8.8

0.0 V
input
i
11111111
ADC

MAX
i
MIN
Motor Enabled